

FIG. 1

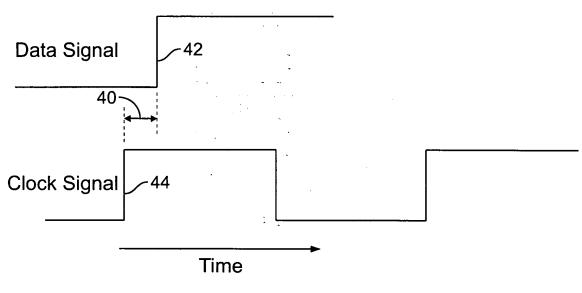


FIG. 2



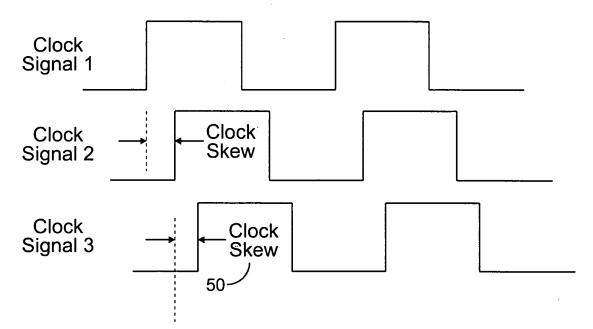
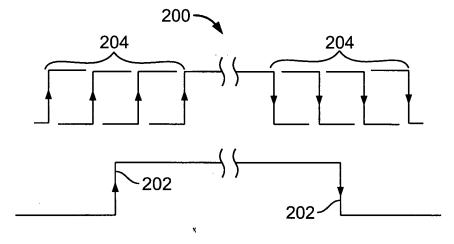


FIG. 3



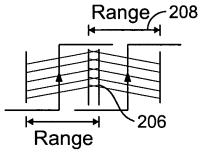
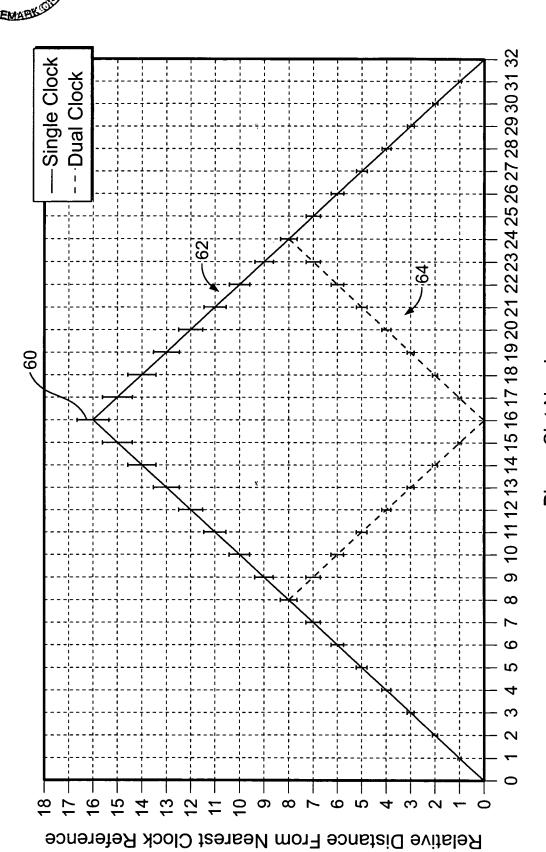


FIG. 4

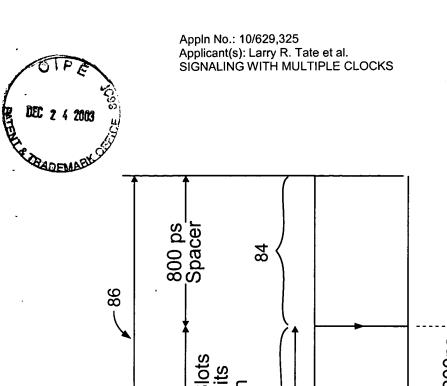


Appln No.: 10/629,325

Applicant(s): Larry R. Tate et al. SIGNALING WITH MULTIPLE CLOCKS

Phase Slot Number

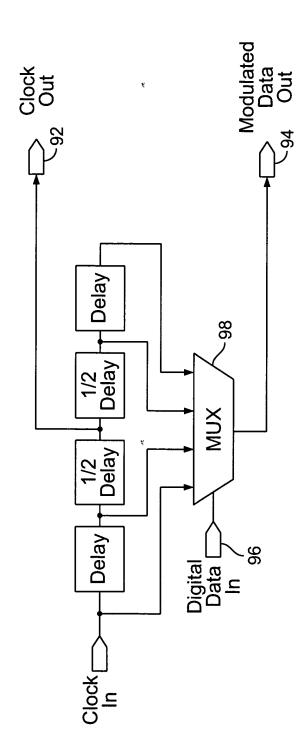
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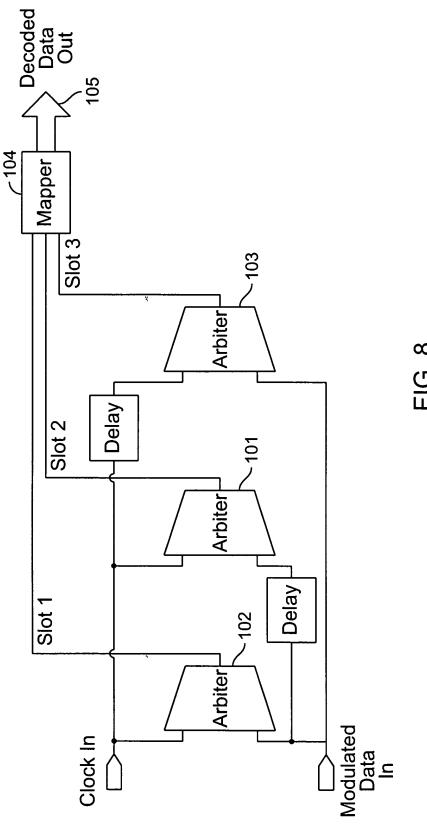
---sd 009--400 ps Phase Slots
800 ps
Provide Two Bits
A Modulation
8200 ps
800 ps
800 ps
Provide Two Bits
8200 ps
800 ps
800 ps
A Modulation
95 Modulation 4000 ps Symbol Frame sd 009 ---• 200ps -2000 ps Clock Pulse -- 600 ps 88 ⊶--- sd 009 ---• 200ps-

FIG. 6

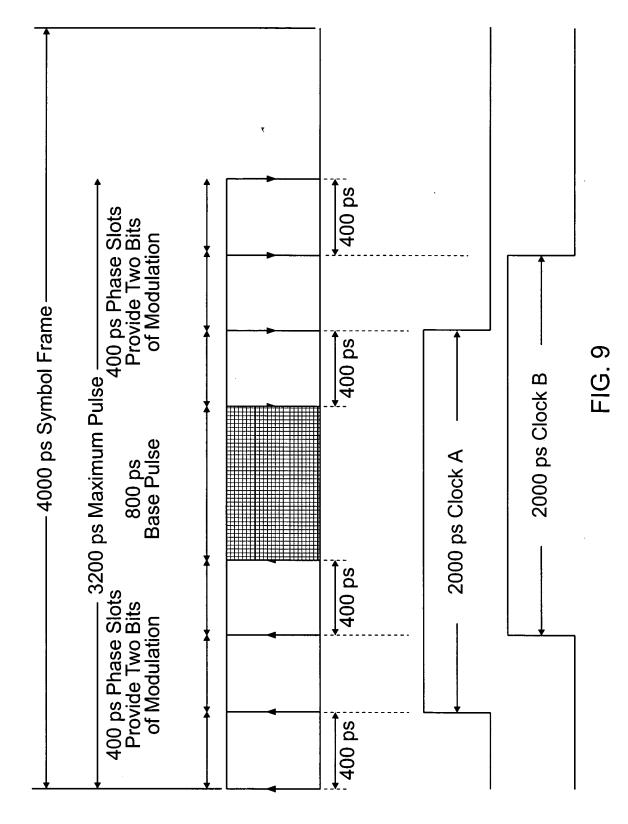














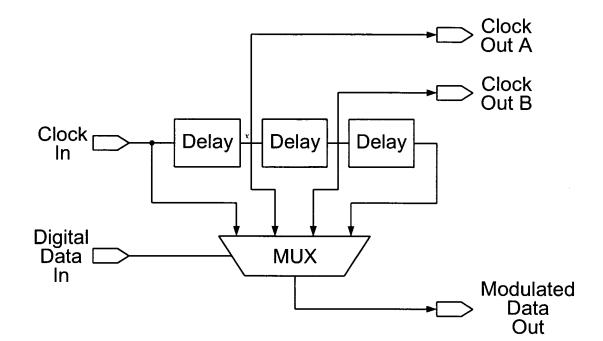
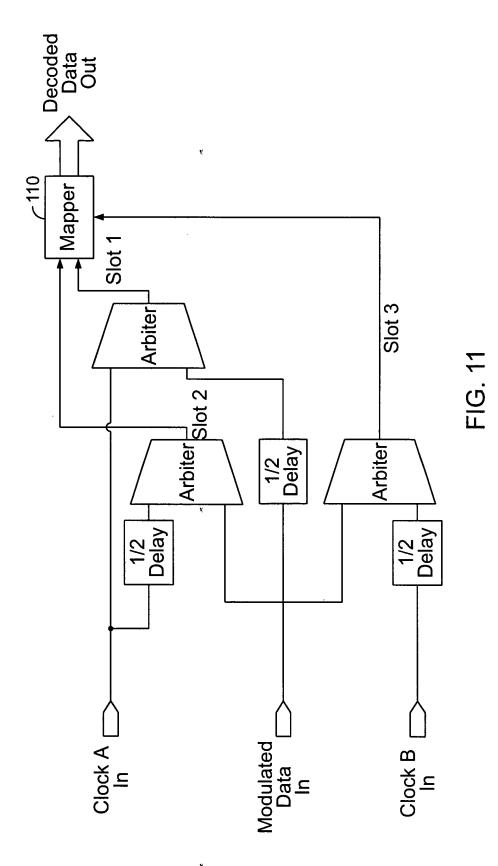


FIG. 10

.DEC 2 4 2003 \* TRADEMARY





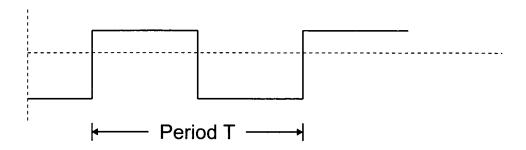


FIG. 12

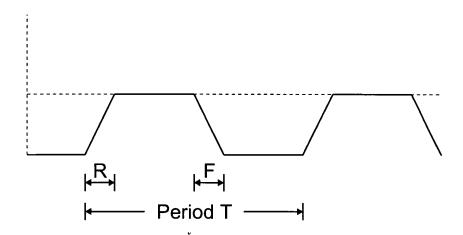


FIG. 13



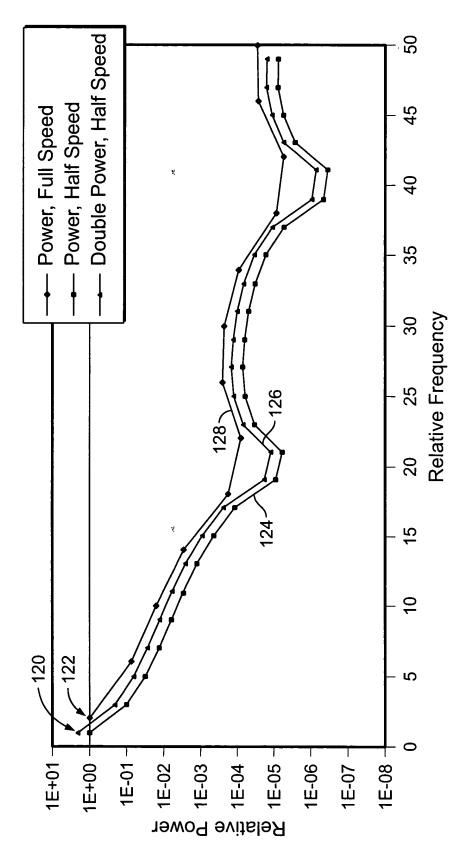
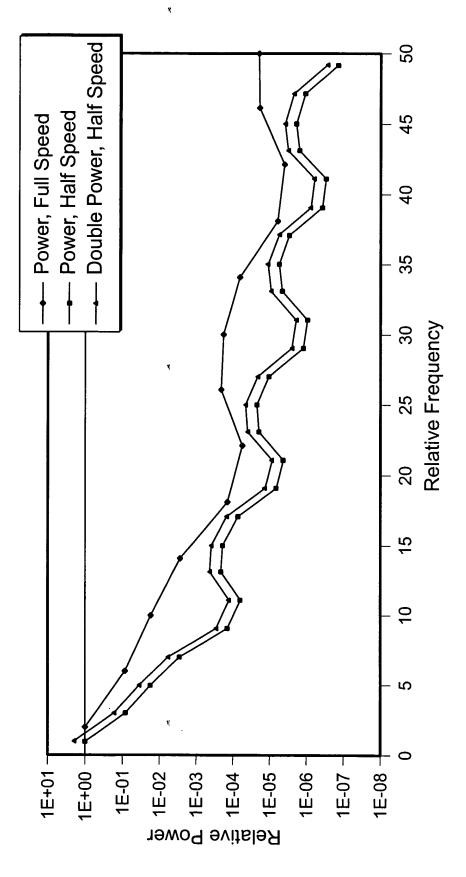


FIG. 14







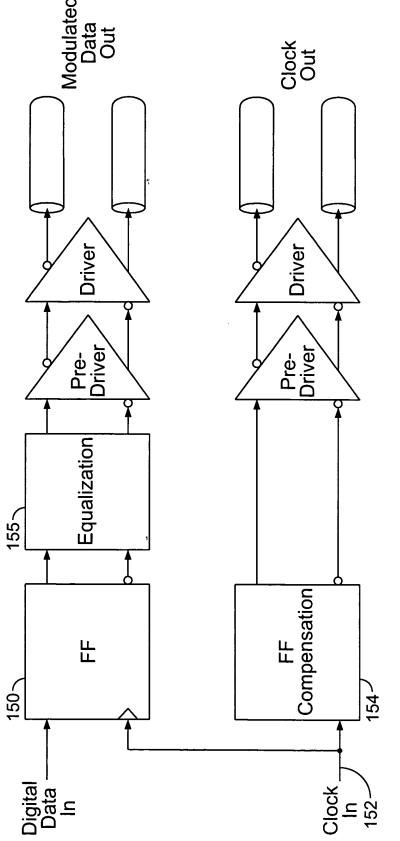
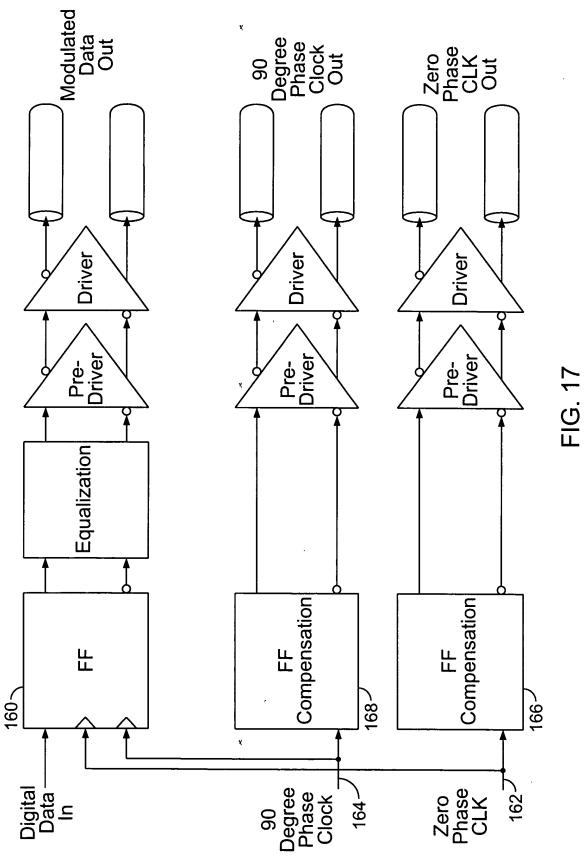


FIG. 16







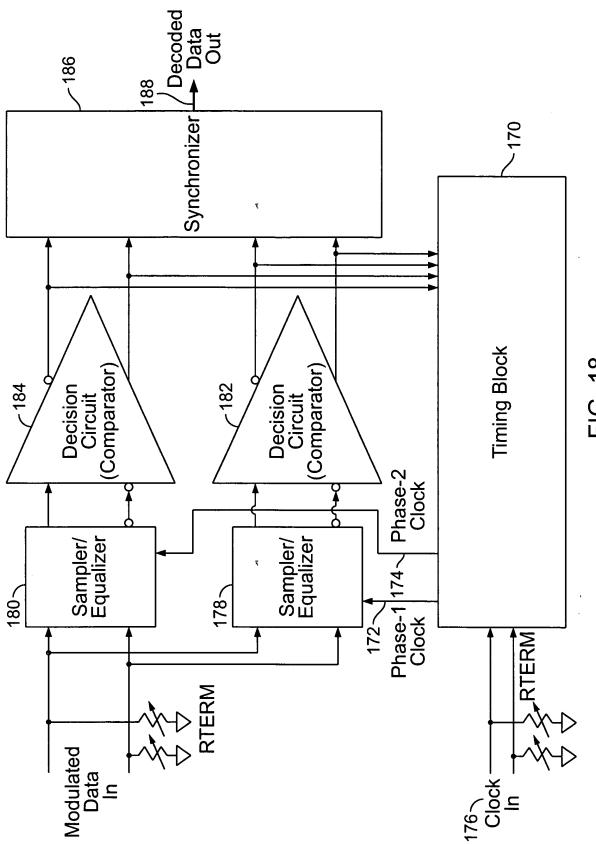


FIG. 18



Decoded ► Data Out Synchronizer -190 Timing Block Decision Circuit (Comparator) Decision Circuit (Comparator) FIG. 19 Phase-2 Clock Sampler/ Equalizer Sampler/ Equalizer 198~ Phase-1 Clock 196~ RTERM RTERM Modulated Data In 90 degree - CLK